REMARKS

Claims 1-29 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Garde (PCT Pub. No. WO 92/08186) in view of Shridhar et al. (U.S. Patent No. 5,381,360). Applicants traverse this rejection because Garde and Shridhar, taken alone or in combination, fail to disclose or suggest a second candidate output value producing unit or means connected for receiving the input value and operable during operation of a first candidate output value producing unit to produce a second candidate output value, or a method of producing a second candidate output value that includes the same features.

The present invention includes mapping circuitry for determining an output value based on a provided input. As shown in Fig. 10 of the present application, the mapping circuitry includes at least a first candidate output value producing unit 42 and a second candidate output value producing unit 44. First unit 42 receives, as inputs, an input value r and a first offset value x. Second unit 44 receives the same input value r and a second offset y. First and second offsets x and y are selected such that the difference between the offsets is equal to the difference between output-range limit values.

Because none of the inputs to first or second candidate output value producing units 42, 44 are dependent upon the output of any other portion of the mapping circuitry, the second candidate output value producing unit can operate to produce a second candidate output value during operation of the first candidate output producing unit. This enables the first and second candidate output values to be available to the

mapping circuitry more quickly than if the first and second candidate output values were produced sequentially.

In other words, both the first and second candidate output value producing units of the present invention receive the provided input. The second unit is operable to produce a second candidate output value while the first output candidate value producing unit is producing a first candidate output value.

In contrast, Garde shows, in Fig. 2, an adder 22 that receives an index value I and an offset M to output an absolute address I+M. After the absolute address is calculated, an adder/subtractor 28 receives the output of the adder 22 and adds/subtracts an offset L to/from that value to generate a wrap address I+M±L. Thus, the adder/subtractor 28 does not receive the index value I. Further, because one of the inputs to the adder/subtractor 28 is the output of adder 22, the adder/subtractor cannot possibly generate its result until after the adder has generated its result. Consequently, Garde does not disclose or suggest a second candidate output value producing unit connected for receiving the input value and operable, during operation of a first candidate output value producing unit, to produce a second candidate output value.

Shridhar does not overcome the above-stated deficiencies of Garde. Shridhar shows, in Fig. 1, two address units 1812, 1814. Each of these address units receives a distinct address and displacement (i.e., address unit 1812 receives address X and a displacement of -1, +1, or the value of one of the registers 1818 or 1820, while address unit 1814 receives address Y and a displacement of +1, -1, or the value of one of

the registers 1860 or 1864). Shridhar fails to disclose any relationship between the displacements selected at this stage of processing. Rather, the displacements are independent of one another.

The output of each of these address units is then stored in respective registers R1. The values stored in the registers R1 are used as inputs to the address units 1812, 1814, along with separate modulo values generated by modulo logic units 1870, 1872 to produce new output values. The output of the address units 1812, 1814 is then stored in respective registers R2.

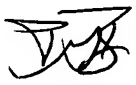
Assuming, *arguendo*, that the values stored by Shridhar in the registers R1 and R2 correspond to first and second candidate output values, respectively, Shridhar still does not disclose or suggest that the address is used as an input to generate the values stored in the registers R2. Instead, as described above, the values stored in R2 are generated based on the values stored in the registers R1 (i.e., the first candidate output value) and modulo values. Further, because the values to be stored in the registers R2 rely on the value stored in the registers R1, the values to be stored in R2 cannot possibly be determined until after the values to be stored in registers R1 have been calculated and stored. That is, the values to be stored in registers R1 and R2 are calculated sequentially, rather than in parallel. Thus, Shridhar also does not disclose or suggest a second candidate output value producing unit connected for receiving the input value and operable, during operation of a first candidate output value producing unit, to produce a second candidate output value.

Therefore, even if Shridhar were combined with Garde, the references would still fail to disclose or suggest a second candidate output value producing unit or means connected for receiving the input value and operable during operation of a first candidate output value producing unit or means to produce a second candidate output value, or a method of producing a second candidate output value that includes the same features. For these reasons, withdrawal of the § 103(a) rejection is respectfully requested.

For all of the foregoing reasons, Applicant submits that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

Patrick G. Burns
Registration No. 29,367

January 14, 2008

300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: 312.360.0080
Facsimile: 312.360.9315

Customer No. 24978